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Claims

[c1] 1.A method of removing silicon dioxide from a surface of a semiconductor device, the method comprising the steps of:
a) reacting the silicon dioxide to form a reaction product on the surface;
b) removing the reaction product from the surface; and
c) annealing the surface.

[c2] 2.The method of claim 1, wherein step (c) comprises annealing in a reducing atmosphere.

[c3] 3.The method of claim 1, wherein the reducing atmosphere comprises hydrogen.

[c4] 4.The method of claim 1, wherein steps (b)-(c) are performed in an oxygen-free ambient to prevent formation of a native oxide layer.

[c5] 5.The method of claim 4, wherein steps (b)-(c) are performed in the same process chamber.

[c6] 6.The method of claim 1, wherein the annealing step (c) comprises a temperature from approximately 700°C to approximately 800°C.

[c7] 7.The method of claim 1, wherein the reacting step (a) comprises a vapor phase etch.

[c8] 8.The method of claim 1, wherein the removing step (b) comprises evaporating the reaction product from the surface.

[c9] 9.A method of forming a vertical bipolar transistor having a single crystal base formed on a substrate, the method comprising the steps of:
a) forming a silicon dioxide layer and a dielectric layer on the base;
b) forming an emitter window in the dielectric layer over the base to expose a portion of
the silicon dioxide layer;
c) reacting the portion of the silicon dioxide layer to form a reaction product layer;
d) removing the reaction product layer from the emitter window to expose a surface of a portion of the base;
e) annealing the substrate; and
f) forming a single crystal emitter on the exposed surface of the base.

[c10] 10.The method of claim 9, wherein the step (e) comprises annealing in a reducing atmosphere.

[c11] 11.The method of claim 10, wherein the reducing atmo-

sphere comprises hydrogen.

[c12] 12.The method of claim 9, wherein steps (d)-(f) are performed in an oxygen-free ambient to prevent formation of a native oxide layer.

[c13] 13.The method of claim 11, wherein steps (d)-(f) are performed in the same process chamber.

[c14] 14.The method of claim 9, wherein the annealing step (e) comprises a temperature from approximately 700°C to approximately 800°C.

[c15] 15.The method of claim 9, wherein the base includes germanium.

[c16] 16.The method of claim 9, wherein the dielectric layer comprises silicon nitride.

[c17] 17.The method of claim 9, wherein the reacting step (c) comprises a vapor phase etch.

[c18] 18.The method of claim 9, wherein the removing step includes evaporating the reaction product from the surface.

[c19] 19.A method of forming an interface between a first single crystal silicon layer and a second single crystal silicon layer, the method comprising the steps of:

a) forming a silicon dioxide layer on the second single crystal silicon layer;

b) reacting at least a portion of the silicon dioxide layer to form a reaction product layer;

c) removing the reaction product layer to expose a surface of the second single crystal silicon layer;

d) annealing the surface; and

e) forming the first single crystal silicon layer on the surface of the second single crystal silicon layer.

[c20] 20.The method of claim 19, wherein the step (d) comprises annealing in hydrogen.